

What Is Claimed Is:

1 1. A method of processing a communications
2 signal comprising:
3 forming a beam in a first direction;
4 roughly determining a direction and end
5 frequency bandwidth of the communications signal to
6 reduce a frequency bandwidth and a range of potential
7 arrivals of said signal; and
8 then forming a beam in a second direction.

1 2. A method of processing a
2 communications signal as recited in claim 1, wherein
3 said first direction is orthogonal to said second
4 direction.

1 3. A method of processing a
2 communications signal as recited in claim 1, further
3 comprising the step of generating a first direction
4 error signal, a second direction error signal, a
5 timing error signal and a frequency error signal.

1 4. A method of processing a
2 communications signal as recited in claim 3, further
3 comprising the step of receiving said first direction
4 error signal and said second direction error signal
5 in a two-dimensional beam forming circuit.

1 5. A method of processing a
2 communications signal as recited in claim 1, further
3 comprising the step of detecting symbols in the
4 signal.

1 6. A method of processing a
2 communications signal as recited in claim 5, further
3 comprising the step of demodulating the signal.

1 7. A method of processing a
2 communications signal, comprising:
3 receiving the signal using $n \times 4$ receive
4 elements, wherein n is an integer at least equal to
5 1, so that each consecutive sample may be offset by
6 90° to avoid cosine and sine multiplications; and
7 forming a beam in a first direction using a
8 fast Fourier transform in a one-dimensional digital
9 beam forming circuit.

1 8. A method of processing a
2 communications signal as recited in claim 7, further
3 comprising the step of reducing the bandwidth of the
4 received signal.

1 9. A method of processing a
2 communications signal as recited in claim 7, wherein
3 forming the beam in a first direction forms columnar
4 fan beams.

1 10. A method of processing a
2 communications signal as recited in claim 9, further
3 comprising the step of applying a correction factor
4 $\Delta\theta_x$ and a frequency correction Δf .

1 11. A method of processing a
2 communications signal as recited in claim 10, further
3 comprising the steps of correcting changes in timing
4 and performing finite impulse response and decimation
5 filtering.

1 12. A method of processing a
2 communications signal as recited in claim 11, further
3 comprising the step of forming the beams in a second
4 direction.

1 13. A method of processing a
2 communications signal as recited in claim 12, wherein
3 the second direction is orthogonal to the first
4 direction.

1 14. A method of processing a
2 communications signal as recited in claim 13, further
3 comprising the steps of correcting at least one of
4 timing errors, phase errors, frequency errors and
5 tracking errors.

1 15. A method of processing a
2 communications signal as recited in claim 14, further
3 comprising the steps of detecting at least one of
4 transmission symbols and characters and performing
5 one or more of demodulation operations to recover
6 data.

1 16. A method of processing a
2 communications signal as recited in claim 15, wherein
3 the demodulation operations comprise signal
4 synchronization, quadrature demodulation, matched
5 filtering, deinterleaving, trellis decoding and
6 unscrambling.

1 17. A method of processing a
2 communications signal as recited in claim 16, further
3 comprising the steps of formatting and handing over
4 the recovered data to a terminal.

1 18. A signal processing circuit
2 comprising:
3 a receive digital signal processing circuit
4 comprising:
5 a receive digital beam forming circuit
6 coupled to nx4 receive elements, wherein n is an
7 integer at least equal to 1, and
8 a transmit digital signal processing
9 circuit comprising:
10 a transmit digital beam forming circuit
11 coupled to nx4 transmit elements, wherein n is an
12 integer at least equal to 1.

1 19. A signal processing circuit as recited
2 in claim 18, wherein the receive elements are
3 partitioned into subarrays of four elements each.

1 20. A signal processing circuit as recited
2 in claim 18, wherein the receive digital beam forming
3 circuit comprises two one-dimensional digital beam
4 forming circuits.

1 21. A signal processing circuit as recited
2 in claim 18, wherein the transmit digital beam
3 forming circuit comprises a two-dimensional beam
4 forming circuit.

1 22. A signal processing circuit as recited
2 in claim 18, wherein the receive digital signal
3 processing circuit further comprises means for
4 filtering.

1 23. A signal processing circuit as recited
2 in claim 18, wherein the receive digital signal
3 processing circuit is coupled to means for
4 controlling power, aiding orientation and velocity.

1 24. A signal processing circuit as recited
2 in claim 18, wherein the transmit digital signal
3 processing circuit is coupled to means for
4 controlling power.

1 25. A signal processing circuit as recited
2 in claim 18, wherein the transmit digital beam forming
3 circuit is coupled to the receive digital signal
4 processing circuit for receiving correction factors.

1 26. A signal processing circuit as recited
2 in claim 18, wherein each of the transmit elements
3 has an associated latch, digital-to analog converter,
4 local oscillator/mixer, beam band pass filter, and
5 amplifier.

1 27. A signal processing circuit as recited
2 in claim 18, said transmit digital signal processing
3 circuit further comprising an encoder/interleave
4 circuit coupled to each of the transmit elements.

1 28. A signal processing circuit as recited
2 in claim 27, wherein each transmit element has a
3 cosine lookup table and a sine lookup table for
4 offsetting each transmit element to represent a phase
5 shift.

1 29. A signal processing circuit as recited
2 in claim 28, said transmit digital signal processing
3 circuit further comprising a summer for summing up
4 converted in-phase and quadrature values.

1 30. A signal processing circuit as recited
2 in claim 29, said transmit digital signal processing
3 circuit further comprising a single digital-to-analog
4 converter and band pass filter.

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1 31. A signal processing circuit
2 comprising:
3 a receive digital signal processing circuit
4 comprising:
5 a receive digital beam forming circuit
6 coupled to an array of 4x4 receive elements, wherein,
7 and
8 a transmit digital signal processing
9 circuit comprising:
10 a transmit digital beam forming circuit
11 coupled to an array of 4x4 transmit element.